CLAIMS

We claim:

1. An integrated circuit device including an isolation region, the device comprising:

an integrated circuit substrate;

a trench in the integrated circuit substrate that defines an active region of the integrated circuit device;

a silicon layer on the integrated circuit substrate and extending over an edge of the trench and along an upper portion of a first sidewall of the trench; and

an insulating material adjacent the silicon layer and extending across at least a portion of the trench to define the isolation region.

2. The integrated circuit device of Claim 1 wherein the silicon layer extending over the edge of the trench defines an overhang that provides an increased area for the corresponding defined active region of the integrated circuit device.

3. The integrated circuit device of Claim 1 further comprising a second silicon layer on the integrated circuit substrate and extending over a second edge of the trench and along an upper portion of a second sidewall of the trench opposite the first sidewall of the trench and wherein the insulating material extends across the trench between the silicon layers.

4. The integrated circuit device of Claim 3 wherein the silicon layers are epitaxial growth layers.

5. The integrated circuit device of Claim 4 further comprising a second insulating layer filling at least a portion of the trench.

6. The integrated circuit device of Claim 5 wherein the silicon layers extending over the edges of the trench define overhangs that extend over the second insulating layer.

7. The integrated circuit device of Claim 5 wherein the upper portions of the sidewalls, along which the epitaxial growth layers extend, have a length between about 400 and about 1000 Angrstroms.

8. The integrated circuit device of Claim 5 wherein the first and second insulating layers comprise the same material.

9. The integrated circuit device of Claim 5 wherein the first insulating layer comprises a high-density plasma (HDP) oxide layer and the second insulating layer comprises a polysilazane oxide layer.

10. The integrated circuit device of Claim 5 wherein the upper portions of the sidewalls, along which the epitaxial growth layers extend, have a length selected to be greater than a depth to which devices are to be formed in the active region.

11. The integrated circuit device of Claim 5 further comprising:

a themal oxide layer along the sidewalls of the trench between the integrated circuit substrate and the second insulating layer; and

a liner between the thermal oxide layer and the second insulating layer.

12. A method for forming an integrated circuit device, comprising:

forming a trench in an integrated circuit substrate to define an active region of the integrated circuit device;

forming a first insulating layer in the trench to a height providing an exposed upper portion on opposing sidewalls of the trench;

forming a silicon layer on the integrated circuit substrate and extending over an edge of one of the sidewalls of the trench and along at least a portion of the exposed upper portion of the one of the sidewalls; and

forming a second insulating layer adjacent the silicon layer and extending across at least a portion of the trench to define an isolation region.

13. The method of Claim 12 wherein the step of forming the silicon layer comprises the step of forming the silicon layer on the integrated circuit substrate and

extending over an edge of each of the sidewalls of the trench and along at least a portion of the exposed upper portion of each of the sidewalls and wherein the step of forming a second insulating layer comprises the step of forming the second insulating layer extending across the trench between the portions of the silicon layer extending over the edges.

14. The method of Claim 13 wherein the silicon layers are epitaxial growth layers.

15. The method of Claim 14 wherein the step of forming a first insulating layer further comprises the step of forming the first insulating layer to provide the upper portions of the sidewalls, along which the epitaxial growth layers extend, a length between about 400 and about 1000 Angrstroms.

16. The method of Claim 14 wherein the first and second insulating layers comprise the same material.

17. The method of Claim 14 wherein the first insulating layer comprises a high-density plasma (HDP) oxide layer and the second insulating layer comprises a polysilazane oxide layer.

18. The method of Claim 14 wherein the step of forming a first insulating layer further comprises the step of forming the first insulating layer to provide the upper portions of the sidewalls, along which the epitaxial growth layers extend, a length selected to be greater than a depth to which devices are to be formed in the active region.

19. The method of Claim 14 further comprising:

forming a themal oxide layer along the sidewalls of the trench between the integrated circuit substrate and the second insulating layer; and

forming a liner between the thermal oxide layer and the second insulating layer.

20. A semiconductor device comprising:

a semiconductor substrate having a trench, which is formed at a predetermined portion of the semiconductor substrate and defines an active region on which devices will be formed;

silicon layers formed to extend from the upper corners of the trench to the upper sidewalls of the trench; and

an insulating layer formed to fill a space between the silicon layers.

21. The semiconductor device of claim 20, wherein the silicon layers are selective epitaxial growth layers.

22. The semiconductor device of claim 20, wherein the silicon layers are grown at the surface of the active region.

23. The semiconductor device of claim 20, wherein the length of the upper sidewalls of the trench is as much as the depth to which devices are formed.

24. The semiconductor device of claim 20, wherein the length of the upper sidewalls of the trench is 400 – 1000 Å.

25. The semiconductor device of claim 20, wherein the insulating layer comprises a first insulating layer for filling a predetermined height of the trench and a second insulating layer for filling the space between the silicon layers.

26. The semiconductor device of claim 25, wherein the first insulating layer is a high-density plasma (HDP) oxide layer.

27. The semiconductor device of claim 25, wherein the second insulating layer is a polysilazane oxide layer.

28. The semiconductor device of claim 25, wherein a thermal oxide layer and a liner are sequentially interposed between the sidewalls of the trench and the first insulating layer.

29. A semiconductor device comprising:

a semiconductor substrate having a trench, which is formed at a predetermined portion of the semiconductor substrate and defines an active region on which devices will be formed;

SEG layers formed on the surface of the active region and at the upper sidewalls of the trench; and

an insulating layer formed to fill a space between the SEG layers formed at the upper sidewalls of the trench,

wherein the length of the upper sidewalls of the trench at which the SEG layers are formed is as much as the depth to which devices will be formed.

30. The semiconductor device of claim 29, wherein the length of the upper sidewalls of the trench at which the SEG layers are formed is 400 – 1000 Å.

31. The semiconductor device of claim 29, wherein the insulating layer comprises a first insulating layer for filling a predetermined height of the trench and a second insulating layer for filling the space between the SEG layers.

32. The semiconductor device of claim 31, wherein the first insulating layer is a HDP oxide layer.

33. The semiconductor device of claim 31, wherein the second insulating layer is a polysilazane oxide layer.

34. The semiconductor device of claim 31, wherein a thermal oxide layer and a liner are sequentially interposed between the sidewalls of the trench and the first insulating layer.

35. A method for manufacturing a semiconductor device comprising:

forming a trench on a semiconductor substrate to define an active region on which devices will be formed;

forming a first insulating layer such that a predetermined thickness of the trench is filled with the first insulating layer;

forming SEG layers by growing the exposed surface of the active region and the sidewalls of the trench to a predetermined thickness; and

filling a space between the SEG layers formed at the sidewalls of the trench with a second insulating layer.

36. The method of claim 35, wherein forming the trench comprises:

sequentially depositing a pad oxide layer and a mask layer on the semiconductor substrate;

patterning predetermined portions of the mask layer and the pad oxide layer; and

forming a trench by etching the semiconductor substrate to a predetermined depth using the patterned mask layer and the patterned pad oxide layer as an etching mask.

37. The method of claim 35 further comprising:

forming a thermal oxide layer at the sidewalls of the trench; and

forming a liner on the thermal oxide layer between the step of forming the trench and the step of forming the first insulating layer.

38. The method of claim 37, wherein forming the first insulating layer comprises:

depositing the first insulating layer such that the trench is sufficiently filled with the first insulating layer;

chemically and mechanically polishing the mask layer, the pad oxide layer, and the first insulating layer so that the surface of the semiconductor substrate is exposed; and

etching the first insulating layer to a predetermined depth such that the upper sidewalls of the trench are exposed,

wherein in etching the first insulating layer, predetermined portions of the thermal oxide layer and the liner are etched.

39. The method of claim 38, wherein the first insulating layer is etched by wet etching.

40. The method of claim 38, wherein the first insulating layer is etched by as much as the depth to which devices will be formed.

41. The method of claim 40, wherein the first insulating layer is etched by about 400 – 1000 Å.

42. The method of claim 35 further comprising:

annealing the semiconductor substrate in a hydrogen atmosphere between etching the first insulating layer and forming the SEG layers or between forming the SEG layers and filling the space between the SEG layers formed at the sidewalls of the trench.

43. The method of claim 42 further comprising forming a thermal oxide layer over the entire surface of the semiconductor substrate after annealing the semiconductor substrate in a hydrogen atmosphere.

44. The method of claim 35, wherein filling the space between the SEG layers with the second insulating layer comprises:

depositing a fluid oxide layer so that the space between the SEG layers is sufficiently filled with the fluid oxide layer;

heat-treating the fluid oxide layer so that the density of the fluid oxide layer is improved; and

etching back the fluid oxide layer.

45. The method of claim 44, wherein the fluid oxide layer is a polysilazane oxide layer.